IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising:

a programmable circuit in which information is programmed;

an information holding circuit which electrically holds information programmed in the programmable circuit;

an internal circuit which operates based on information held in the information holding circuit;

a compression circuit which compresses the information held in the information holding circuit;

an information output circuit which outputs expected value information; and

a detecting circuit which compares the expected value information with compression information of the information compression circuit to check destruction of information held in the information holding circuit, when the internal circuit operates.

Claim 2 (Original): The device according to claim 1, further comprising a correction process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that the information is destroyed.

Claim 3 (Currently Amended): The device according to claim 2, wherein the information programmed in the programmable circuit is tested before initiating a correction process, the correction process [[is]] being a process to transfer information programmed in the programmable circuit to the information holding circuit when the information held in the information holding circuit is detected as destroyed.

Claim 4 (Original): The device according to claim 2, further comprising a mirror-ring information holding circuit configured by connecting the information holding circuit in a mirror-ring form, wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit.

Claim 5 (Original): The device according to claim 2, further comprising an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro,

wherein the correction process execution circuit suspends a system containing the IP macro when the IP macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status.

Claim 6 (Original): The device according to claim 1, wherein the information output circuit includes an expected value information generating circuit which generates expected value information and the expected value information generating circuit compresses information programmed in the programmable circuit to generate expected value information when the programmed information is held in the information holding circuit.

Claim 7 (Original): The device according to claim 6, wherein the compression process is an accumulative addition process.

Claims 8-19 (Canceled).

IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 4, 5, and 6. These sheets, which include Figs. 4, 5, and 6, replace the original sheets including Figs. 4, 5, and 6.

Attachment: Replacement Sheets